REMARKS

Claims 1-36 are pending. Claims 1 and 30 are independent claims.

The examiner rejected claims 1-29 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. More specifically, the examiner cannot find support for an "inactive thread."

The examiner also rejected claims 1-29 under 35 U.S.C. §112, second paragraph.

Applicant has amended claims 1 and 30. No new matter has been added. Support for the amendments is included in the detailed description as originally filed:

> By employing hardware context swapping within each of the micro engines 22a-22f, the hardware context swapping enables other contexts with unique program counters to execute in that same micro engine. Thus, another thread, e.g., Thread_1 can function while the first thread, i.e., Thread_0, is awaiting the read data to return. During execution, Thread_1 may access the SDRAM memory 16a. While Thread_1 operates on the SDRAM unit 16a, and Thread_0 is operating on the SRAM unit 16b, a new thread, e.g., Thread_2 can now operate in the micro engine 22a. Thread_2 can operate for a certain amount of time until it needs to access memory or perform some other long latency operation, such as making an access to a bus interface. Therefore, simultaneously, the processor 12 can have a bus operation, SRAM operation and SDRAM operation all being completed or operated upon by one micro engine 22a and have one more thread available to process more work in the data path. (Page 3, lines 30-32 to page 4, lines 1-10)

Accordingly, claims 1-29 are proper under 35 U.S.C. §112, first paragraph, and 35 U.S.C. §112, second paragraph.

The examiner uses Agarwal to reject claims 1-23, 26 and 30-36 as having been anticipated.

Applicant has amended claims 1 and 30 to recite "...causing the ALU to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting," or similar language. Agarwal neither describes nor suggests at least this quoted claim feature.

The examiner misplaces his reliance on Agarwal by arguing the ctx_swap parameter disclosed in applicant's detailed description. The examiner fails to recognize that no such ctx_swap parameter limitation is contained in claims 1 and 30, and that the ctx_swap parameter is an optional parameter, as clearly described in applicant's original detailed description, i.e., "(a) format of the instruction that issues a memory reference to SRAM is sram[sram_cmd, $sram_xfer_reg, source_op1, source_op2, ref_count_or_queue_num_or_bit_op], optional_token." (page 11, lines 3-6) No ctx_swap parameter is required for this instruction.

Agarwal discloses a processor architecture that allows rapid context switching using multiple register sets on the processor. (see page 3, col. 2, last paragraph) Agarwal's architecture is referred to as APRIL. "APRIL continues executing a single thread until a memory operation involving a remote request (or an unsatisfactory synchronization attempt) is encountered." (see page 4, col. 1, third paragraph) Agrawal discloses an instruction set included with APRIL on page 6, and memory instructions on page 6, col. 2, second paragraph. No memory instruction is disclosed or suggested in Agrawal as recited in applicant's claims 1 and 30.

The examiner argues that the SPARK processor of Agrawal includes "...threads capable of making memory requests to a distributed, globally-shared memory." (see office action, page 4, lines 4-5)

Applicant agrees that SPARK, as well as a plethora of processors, are capable of making requests to a memory. However, applicant's claimed invention recites causing the ALU to issue a memory reference to an address in a memory shared among threads executing in the microengines while a context of a thread is waiting. Applicant's invention concerns multiple threads executing in multiple microengines, while Agrawal discloses merely a single SPARK-based processor that supports four hardware contexts (page 2, col. 1, first paragraph).

Accordingly, claims 1 and 30 cannot be (and are not) anticipated by Agrawal.

The examiner uses Agrawal to reject dependent claims 24, 25 and 27-29 as having been obvious.

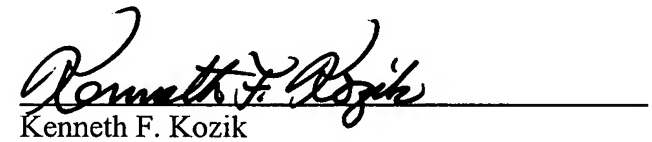
Claim 1 is not rendered obvious by Agrawal. Claims 24, 25 and 27-29 depend upon, and add further limitations to claim 1, Accordingly, claims 24, 25 and 27-29 are not rendered obvious by Agrawal.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: January 5, 2005



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